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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,664	11/16/2001	Andrew J. Castellano	BP1519	8496
34399	7590	05/03/2005	EXAMINER	
GARLICK HARRISON & MARKISON LLP			TRAN, KHAI	
P.O. BOX 160727				
AUSTIN, TX 78716-0727			ART UNIT	PAPER NUMBER
			2637	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/992,664

Applicant(s)

CASTELLANO ET AL.

Examiner

KHAI TRAN

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-76 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 45-62, 75 and 76 is/are allowed.
- 6) ☒ Claim(s) 1, 2, 5, 6, 11, 14-16, 18, 19, 21, 22, 26, 29-34, 39-41, 43, 44, 63, 70, 71, 73 and 74 is/are rejected.
- 7) ☒ Claim(s) 3, 4, 7, 8, 9, 10, 12, 13, 17, 20, 23, 24, 25, 27, 28, 35, 36, 37, 38, 42, 65, 66, 67, 68, 69, 72 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: ***

Page 9, lines 16-19, the term "internal registers 435 or 430" should be changed to –internal register 445—and the term "external registers 435" should be changed to –external register 430--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

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consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-2, 5, 6, 11, 14, 15, 16, 18, 19, 21, 22, 26, 29, 30, 31, 32, 33, 34, 39, 40, 41, 43, 44, 63, 64, 70-71, 73-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Umemura et al (U.S. Pat. 6,088,829) in view of Voit (U.S. Pat. 6,510,473).

Regarding claims 1, 6, Umemura et al disclose an inter-device adaptable interfacing clock skewing system, comprising: a first device (401); and a second device (400) is communicatively coupled to the first device; and wherein the first device comprises a clock generation circuit (an oscillation unit for generating clock signal, col. 3, lines 40-45) for selecting and providing a clock signal to the second device, the clock signal having a frequency and a phase (col. 3, lines 40 to col. 4, line 26). Umemura et al fail to disclose the first device further comprising a pin that is used to select at least one of the frequency of the clock signal and the phase of the clock signal that is provided to the second device.

Voit discloses a selection control pin (120) in a clock circuit (100) used to select at least one of the frequency of the clock signal and the phase of the clock signal (col. 4, line 54 to col. 5, line 10). It would have been obvious to one having ordinary skill in the art at the time invention was made to select the frequency and phase of the clock signal as taught by Voit into the teaching of Umemura et al for providing a desired clock frequency to the second device.

Regarding claim 2, Voit discloses the second device selecting the pin (a peripheral component interconnect (PCI) slot 106, see Fig. 2).

Regarding claim 5, Umemura et al disclose a register containing within the first device (see Figure 10).

Regarding claim 11, Umemura et al disclose the first device comprising phase locked loop (PLL) operable to perform phase shifting of the clock signal before the clock signal is provided to the second device (col. 19, lines 52-63).

Regarding 14, Umemura et al disclose wherein the second devices providing at least one additional clock signal to the first device (see Figure 10).

Regarding claim 15, Umemura et al disclose wherein the second device providing data to the first device (see Figure 10).

Claims 16, 18, 21 are similar to claims 1 and 5. Therefore, claims 16, 18, 21 are rejected under a similar rationale.

Claim 19 is similar to claim 2. Therefore, claim 19 is rejected under a similar rationale.

Claim 22 is similar to claim 6. Therefore, claim 22 is rejected under a similar rationale.

Claim 26 is similar to claim 11. Therefore, claim 26 is rejected under a similar rationale.

Claim 29 is similar to claim 14. Therefore, claim 29 is rejected under a similar rationale.

Claim 30 is similar to claim 15. Therefore, claim 30 is rejected under a similar rationale.

Claim 31, 33, 34, 40 are similar to claim 1. Therefore, claims 31, 33, 34, 40 are rejected under a similar rationale.

Regarding claims 32, Umemura et al disclose the phase difference comprising one zero and 90 degrees (col. 17, line 33-46).

Claim 39 is similar to claims 5 and 21. Therefore, claim 39 is rejected under a similar rationale.

Claim 41 is similar to claim 2. Therefore, claim 41 is rejected under a similar rationale.

Claim 43 is similar to claim 11. Therefore, claim 43 is rejected under a similar rationale.

Claim 44 is similar to claim 15. Therefore, claim 44 is rejected under a similar rationale.

Claim 63 is similar to claim 31. Therefore, claim 63 is rejected under a similar rationale.

Claim 64 is similar to claim 32. Therefore, claim 64 is rejected under a similar rationale.

Claims 70-71 are similar to claim 1. Therefore, claims 70-71 are rejected under a similar rationale.

Claims 73-74 are similar to claims 43-44. Therefore, claims 73-74 are rejected under a similar rationale.

Allowable Subject Matter

5. Claims 45-50, 51-62, 75-76 are allowed.
6. Claims 3, 4, 7, 8, 9, 10, 12, 13, 17, 20, 23, 24, 25, 27, 28, 35, 36, 37, 38, 42, 65, 66, 67, 68, 69, 72 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
7. The following is a statement of reasons for the indication of allowable subject matter: Umemura et al and Voit fail to disclose the second device comprising a clock skewing circuitry, the clock skewing circuitry being operable to skew a received clock signal to generate a skewed clock signal, the received clock signal being transmitted by the first device and received by the second device and skewed clock signal having a received frequency and received phase; the first device further comprising a first pin that is used to select at least one of the frequency of the transmitted clock signal and the phase of the transmitted clock signal that is provided from the first device to the second device; and the second device further comprising second pin that is used to select at least one of the frequency of the skewed clock signal and the phase of the clock signal that is generated within the second device.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ueno et al (U.S. Pat. 5,08,831) disclose a network interface system.

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Sung et al (U.S. Pat. 6,408,831) disclose a phase-locked loop circuitry for programmable logic devices.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAI TRAN whose telephone number is (571) 272-3019. The examiner can normally be reached on 7:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JAY PATEL can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



KHAI TRAN
Primary Examiner
Art Unit 2637

KT
April 27, 2005